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V128 General Purpose VME I/O Module Specification

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V128 General Purpose VME I/O Module System Specification

1.0 Overview

This document describes the design issues of the V128 general purpose VME I/O module. This module has the following features:

1. There are eight outputs, four inputs and four I/O on the front panel. On-board jumpers can configure the four I/O ports as inputs or outputs. These inputs and outputs are all TTL logic with 50Ω impedance. The inputs can be photo-isolated. The relationship between the inputs and outputs are determined by an IO PLD.

2. The input-output relation is controlled by an IO PLD (Altera Flex10K10). This IO PLD can be configured with VME downloaded gate array files through VME read/write operations. Different versions of VME downloaded gate array files define the different relationship between the outputs and the inputs. This feature allows us to configure the IO PLD without taking the board or the PLD out of the system.

3. There are 32 8-bit read/write registers accessible through VME bus on the IO PLD. The values of these registers can be changed dynamically through VME read/write operations without configuration of the whole PLD. These registers provide some convenience for applications in which some VME read/write registers are needed. For example, some applications may need to use these registers as software inputs or use them to save input values.

There are many possible definitions of the input-output relationship through different version of gate array files. Since the files can be downloaded through VME bus, the switching between different versions of files are flexible.

2.0 Front panel Layout

The V128 front panel layout is shown in ***figure 1***. The following paragraphs give descriptions of the front panel LEDs.

VME SELECT

This LED is flashed ON when the module has completed a VME cycle. The on-board DTACK or BERR signals are used to trigger this LED.

VME FLASH

This LED is flashed ON when the on-board flash memory is accessed through VME bus operations. When the flash is erased, written or read, this LED is flashed ON.

CONFIG IOPLD

This LED indicated that the IO PLD is in the process configuration using the configuration file saved in the on-board flash memory.

VME IOPLD

This LED is flashed ON when the IO PLD registers are read/write through VME bus.

OUT [1..8]

These LEDs indicted that there is a HIGH TTL output signal in the corresponding port.

IO [1..4]

These LEDs indicated that there is a HIGH TTL output signal when the corresponding port is configured as an output port or there is a HIGH TTL input signal when the corresponding port is configured as an input port.

IN [1..4]
These LEDs are flashed ON when the corresponding input signal is a HIGH TTL input signal.

3.0 Block Diagram

A block diagram of the V128 module is shown in ***figure 2.***

4.0 VME Memory Map

Address modes:
39: standard (24-bit address) nonprivileged data access;
3d: standard (24-bit address) supervisory data access.

Data transfer modes:
D08(OE)

A24 address space

256Kbyte boundary is assigned to the board and it is selected via dip switched for vmea[23..18].

The following table defines the VME memory regions for the V128 module.

Address Range	Description	Add mode / Data mode	Size (actual used)
00000 - 03fff	ID ROM	39,3d / D08(OE)	16 Kbytes (64 byte uses)
04000 - 07fff	VME Interface Registers	39,3d / D08(OE)	16 Kbytes (1 bytes)
08000 – 0800f	IO PLD Registers: Application related	39,3d / D08(OE)	16 byte (depend on IO PLD version)
08010 – 0801f	IO PLD Registers: IOPLD infomation (name, version)	39,3d / D08(OE)	16 byte (depend on IO PLD version)
20000 - 3ffff	Flash Memory	39,3d / D08(OE)	128 Kbytes (for IO PLD configuration file .rbf, the last 256 bytes used for IO PLD version comments)

5.0 VME Memory and Register Definitions

5.1 ID ROM

The VME ID is 64-byte each and has the standard format established for RHIC VME boards. The even bytes are all ASCII "." (0x2E). The odd bytes give the information of the board and PLD name, version, etc.

5.2 VME Interface Registers

These registers are used to save the VME interface information such as command register to start configuration of IO PLD, error status, etc.

04000: write Start IO PLD configuration command register
This is the command register to trigger IO PLD configuration using the data saved in flash memory. To start the configuration process, 0xAA should be written to this register.

5.3 IO PLD Registers

There are 32 8-bit read/write registers on IO PLD reserved for each version of IO PLD gate array file. The values of these registers can be changed dynamically through VME read/write operations. These IO PLD registers are version-dependent and are defined in different PLD gate array files. Some applications may need to use these registers as software inputs or use them to save input values. These registers are IO PLD version depended and are defined in different application specifications. Always reserved the second 16 bytes for information of IOPLD (name of IOPLD and version).

5.4 Flash Memory

The flash memory is used to save the configuration file for the IO PLD. The flash memory chip is AM29F010B, AMD 5volt bulk erase flash memory. The memory capacity is 128Kbytes. The read, write and erase of the flash memory are done through a few VME bus read/write cycles. The addressing of the memory is through vme_address[17..1]. Data bus is 8 bits wide.

6. Ground Issues

All the IO ports use LEMO connectors and signal coaxial cable. Ground issues play an important role in this module. The ground connections should provide isolation between the two units connected by a cable and should also avoid introducing noises to signals.

6.1 Output ports

The shells of LEMO connectors are connected to the ground of the front panel (chassis ground) instead of connected to the board ground (digital ground or VME bus gorund). Such arrangement helps to avoid connecting the digital ground to a remote ground, which may not have the same voltage level as the digital ground.

A CGND_DGND jumper provides the option to connect the chassis ground and digital ground together.

6.2 Input ports

The shells of LEMO connectors are connected to the chassis ground through a capacitor. A jumper can also directly connect each input LEMO shell to the chassis ground. The input signals can be photo-isolated by jumpers if necessary.

6.3 IN/OUT ports

The shells of LEMO connectors are connected to the chassis ground.

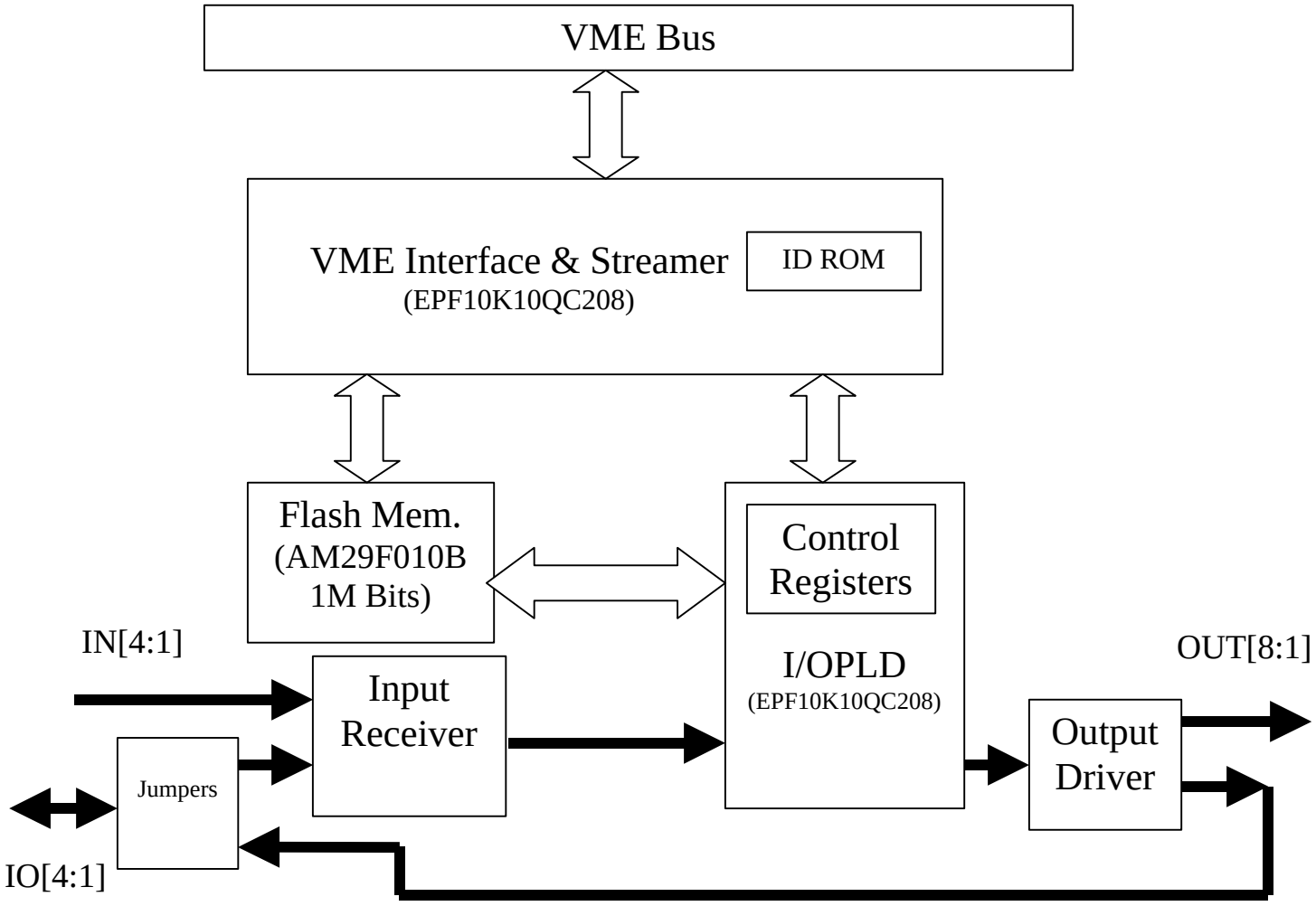

Figure 1 Block diagram of V128 module

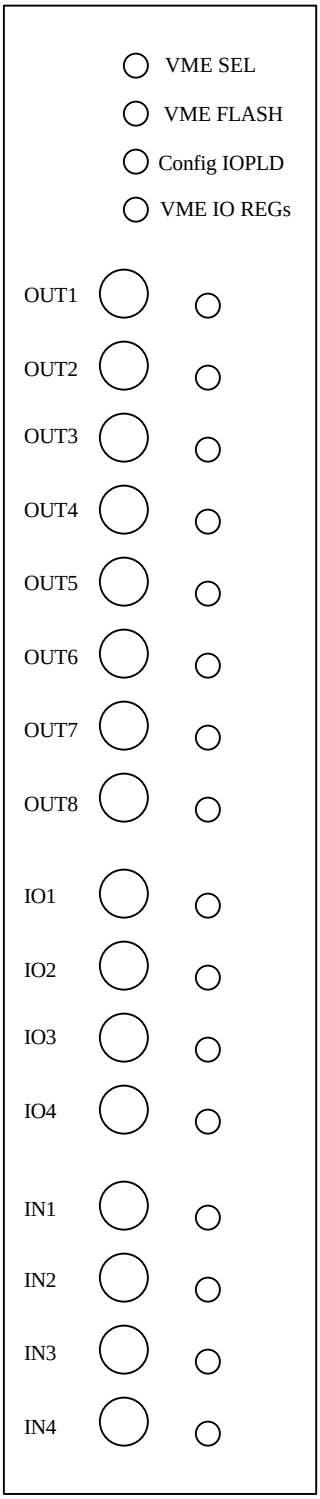

Figure 2. Front panel of V128 module